Advanced Active Deep Trench Designs for Enhanced Charge Transfer Performances in CCD-on-CMOS Image Sensor

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***Abstract* – New designs of active deep trench (CDTI) CCD-on-CMOS are described and characterized: A two-phase pixel with a built-in electric field, enabling highly efficient charge transfer with minimum dark current, and a novel four-phase pixel. The effects of pixel pitch and transfer time are discussed.**

I. Introduction and Context

The development of high-performance CCD-on-CMOS is of strategic importance for a large number of applications taking profit from Time Delay Integration (TDI) imaging. The low-noise charge binning capability, inherited from CCDs, can be cumulated with the CMOS process benefits: ease of integration, access to advanced tech nodes, low-power dissipation, and any combination of CMOS functions with stacking possibilities. In this framework, a 2-phase CDTI-based CCD-on-CMOS has been introduced in 2020 [1] with promising charge transfer performance, high dynamic range, and notable radiation hardness [2] thanks to the use of low biases and a specific dither clocking enabling multi-pinned phase (MPP) charge transfer by dynamic trench passivation.

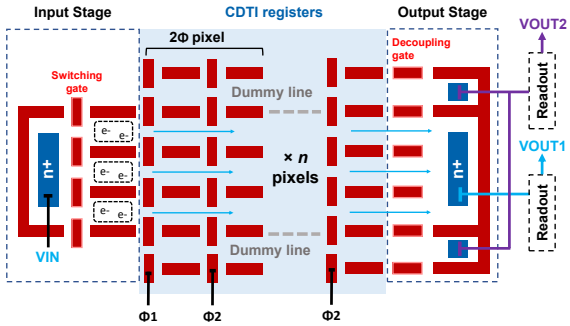

Fig. 1: Schematic of the studied test structure. It features n pixels (3 sub-columns) enclosed between a common input and output stage (VOUT1). On the sides, dummy lines are featured (VOUT2).

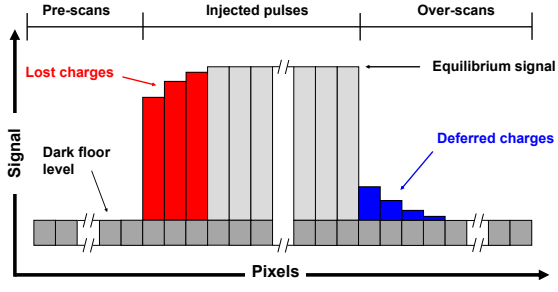

Fig. 2: Sketch of the CTI measurement showing the dark background and both lost and deferred electrons. A comparison with the equilibrium signal gives the fractional loss per pixel.

This work reports improved CCD-on-CMOS designs, based on a BSI technology with active deep trench, taking profit of the CDTI vertical MOS to further improve the charge transfer efficiency (CTE). Two new designs are assessed: a two-phase pixel with "trapeze" shaped CDTI yielding a built-in electric field, and a four-phase pixel for buried channel improvements.

One key target is to explore the potential of such improved pixels for multi-spectral TDI Earth observation detectors, which feature panchromatic and spectral bands potentially covering a large range of pixel pitches and respective transfer frequencies (typically $\geq 10\,\text{kHz}$). However, the potential applications are not limited to remote sensing. For instance, enhancing charge transfer in large pixels could greatly benefit various scientific and medical applications [3]. Furthermore, achieving high line rate operations ($\geq 1\,\text{MHz}$) would pave the way for TDI-based industrial machine vision and defect inspection applications [4].

As such, this paper investigates charge transfer inefficiency (CTI) in these new CCD-on-CMOS active deep trench pixel designs with pitches spanning from 6 µm up to 48 µm under various transfer time constraints.

II. Experimental Details

Fig. 1 shows a schematic of the test structure. It features a column of n pixels composed of three sub-columns connected to a common input and output stage employed for CTI measurements. Two dummy lines, on each side of the main register, are also read out to monitor charge blooming. CTI is estimated by injecting some signal pulses and integrating the average of the lost and deferred charges (EPER and FPER methods) in a single sequence, as shown in Fig. 2. In the following, each reported CTI value represents the average measurement obtained from two independent test structures.

III. Trapeze-shaped CDTI gates to yield a built-in electric field

In Fig. 3, the new design featuring a built-in-pixel electric field is exhibited. This field is induced by the "trapeze" shape of the CDTI gates creating a channel width gradient, causing the depletion potential to increase gradually toward the charge transfer direction. This design has the benefit of requiring only an adaptation of the CDTI layout compared to other methods involving a doping gradient to achieve a similar built-in electric field effect [5], [6]. If α is the width gradient and W_0 the minimum channel width, then the electric field along x, in full depletion is:

$$E(x) = -\frac{N_d q}{4\epsilon}(\alpha^2 x + \alpha W_0) \quad (1)$$

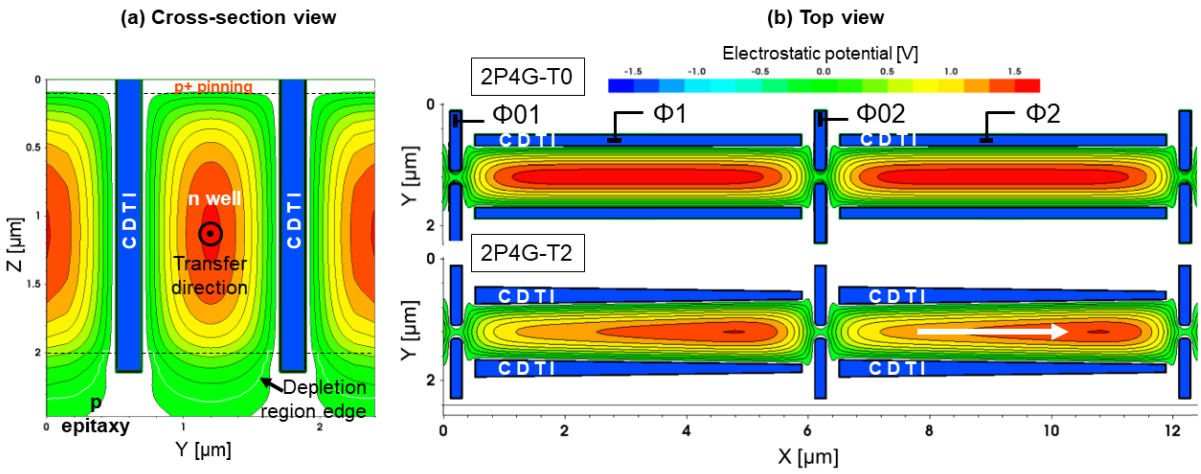

Fig. 3: On (a) is the cross-section of one sub-column in the middle of a phase, showing the channel depth. On (b) is the top view potential map of a reference pixel (2P4G-T0) and a trapeze pixel (2P4G-T2). The built-in electric field in the 2P4G-T2 is exhibited. In this simulation, every CDTI gate is biased at –1V. The 2D TCAD simulations are performed with Synopsys Sentaurus 2020.09-SP1 Software.

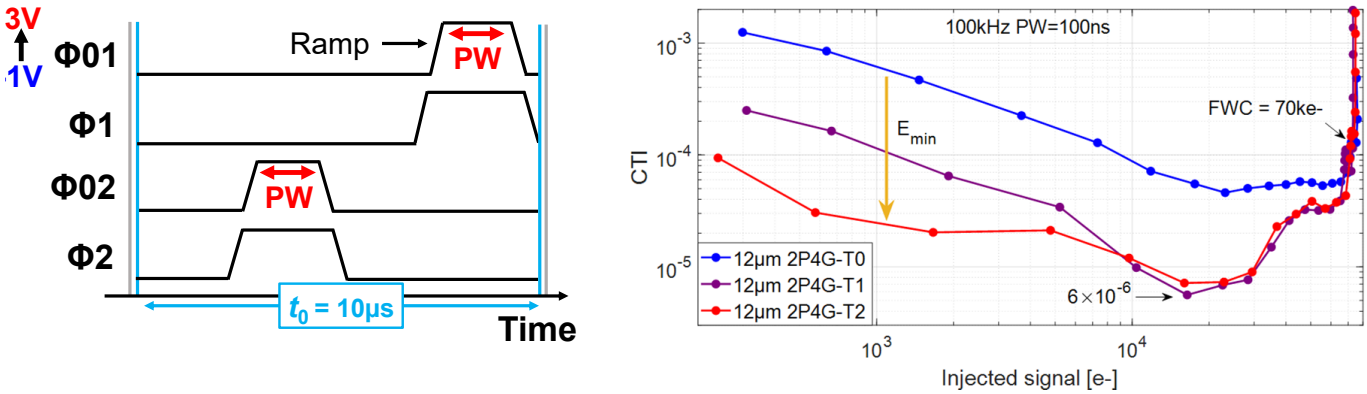

Fig. 4: On the left is a typical 2P4G clocking diagram. The TCDTI phase pulse (Φ01 and Φ02) is slightly shorter than the CDTI phase pulse (Φ1 and Φ2) to account for the smaller capacitance inducing faster phase switching. On the right is the CTI measured at 100 kHz with PW=100 ns versus the injected signal in the case of 2P4G-T0, 2P4G-T1, and 2P4G-T2.

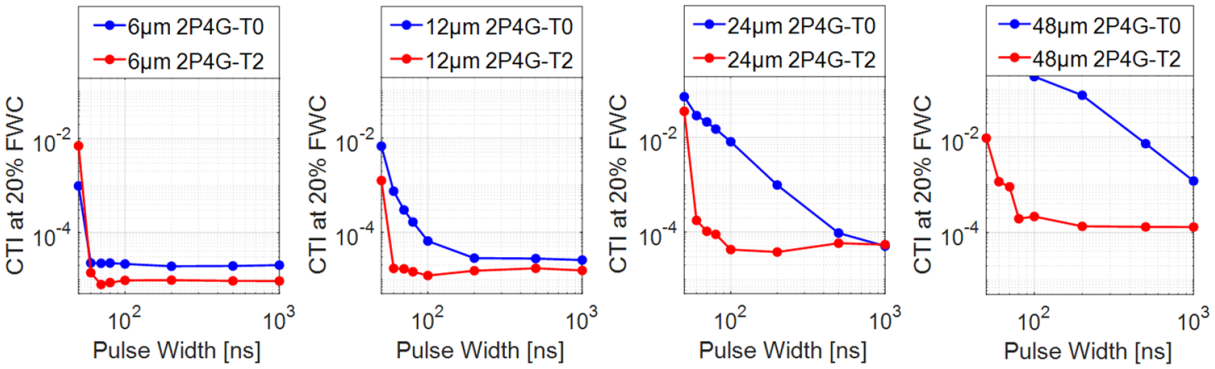

Fig. 5: CTI at 20% FWC versus PW and compared between 2P4G-T0 and 2P4G-T2 with pixel pitches 6 µm, 12 µm, 24 µm and 48 µm.

With N_d the doping concentration and ϵ the silicon dielectric constant. For example, in a 6 µm phase as in Fig. 3, the trapeze version yields a mean electric field of $1\,\mathrm{kV/cm}$, enabling an electron to travel from end to end in less than a ns. This concept intends to facilitate low-signal transfers by gathering the electrons close to the transverse CDTI (TCDTI) gates while the transfer pulse has not yet occurred. Hence, the mean transfer distance is reduced, and fringing field drift is maximized, enabling transfer to happen in a shorter time. The built-in field effect is expected to fade out for increasing signals in favor of the self-induced drift mechanism.

In Fig. 4, the CTI is measured at a frequency of 100 kHz and a transfer pulse width (PW) of 100 ns in a reference 2-Phase 4-Gate device (2P4G-T0), in a lightly trapeze-shaped device (2P4G-T1) and a strongly trapeze-shaped device (2P4G-T2), each with 220 pixels of 12 µm long. A CTI reduction can be seen with the introduction of trapeze CDTI, with the best improvement at low injection. The difference between 2P4G-T1 and 2P4G-T2 is only noticeable for signals below 10 ke-. While exceptionally low levels of CTI are attained (6×10^{-6}), only a light Full Well Capacity (FWC) decrease is observed, making it an acceptable trade-off.

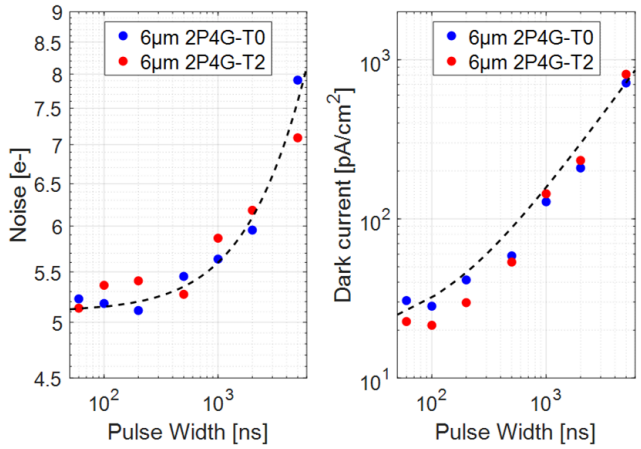

Fig. 6: Output noise and dark current density versus PW. Both are measured when applying the clocking diagram shown in Fig. 4.

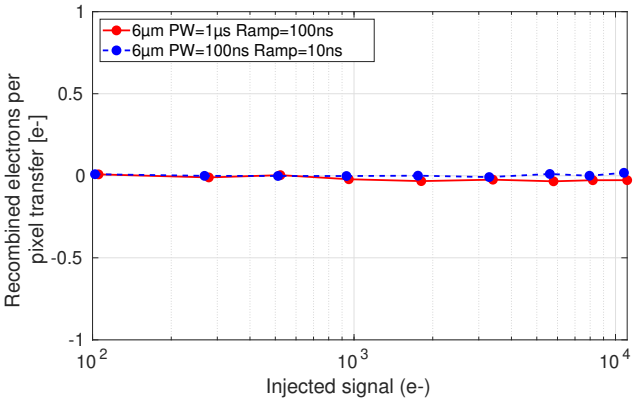

Fig. 7: Recombined charges at the TCDTI interface per pixel transfer as a function of transfer pulse clock.

In Fig. 5, the CTI improvement is generalized to various pixel pitches from 6 µm to 48 µm by comparing 2P4G-T0 and 2P4G-T2 at 20% FWC. While trapeze CDTI improves CTI in every case, the effect is more pronounced for longer pitches due to increased travel distance. With the clock swing set to $[-1\mathrm{V}; 3\mathrm{V}]$, a PW of 60 ns appears to be the lower limit for charge transfer investigation. Below this threshold, trench gate capacitive effects may prevent complete phase switching, thus blocking charge transfer despite the fringing field extension. The reason why CTI improves in 6 µm 2P4G-T2 pixels for any PW is unclear and results probably from a CTI artifact. One can conclude the trapeze process is most useful in large pixels, with significant CTI improvements in 12 µm pixels for PW $\leq$ 200 ns, in 24 µm pixels for PW $\leq$ 500 ns and in 48 µm pixels for PW $\leq$ 1000 ns at least.

The fact that transfer time can be set in the hundreds of ns range while keeping CTI low is very encouraging for high line rate operations. Moreover, it enables further optimization of the MPP mode by improving the CDTI active passivation feature. With PW = 100 ns, transfer time is about 10^5 times faster than the average interface trap emission lifetime at 300 K. As can be seen in Fig. 6, it results in very low dark current ($25\,\mathrm{pA.cm^{-2}}$) and minimum noise ($5\,\mathrm{e^-}$). The 6 µm 2P4G-T0 and 2P4G-T2 exhibit similar characteristics despite the process change. It shows the trapeze pixel version combines both low dark current and efficient charge transfer.

In previous works, the TCDTI gates have been suspected as potential CTI causes and charge recombination centers due to their proximity with the signal during charge transfer like several localized surface channels [2]. It has been demonstrated that a TCDTI gate can be employed as a clocked anti-blooming system by pumping charges at its interface [7]. In this study, this effect is evaluated by comparing the signal output when the TCDTI is biased in inversion mode (-1 V), promoting charge recombination, to the signal output when the TCDTI gate remains un-inverted (0.5 V), where recombination is prevented. A subtraction shows the output signal is in fact very similar no matter the TCDTI bias. In Fig. 7, the recombined electrons per pixel transfer are shown with respect to the injected signal in 6 µm pixels, using transfer pulse widths of 100 ns and 1000 ns. This result indicates that interface recombination does not occur along the TCDTI path, even with very fast phase switching. Consequently, it is not a limiting factor for high-frequency applications.

IV. Toward a four-phase pixel design with improved buried channel properties

An alternative design, composed of four phases (4P4G), is tested to assess the CTI in a TCDTI-less device. This design aims to evaluate whether the TCDTI gates, specific to the two-phase architecture, inherently hinder CTE and, in this eventuality, whether sacrificing the MPP feature of the two-phase design is worth the CTE gain.

A top view of a 12 µm pixel is shown in Fig. 8 in the case of charge storage performed under two phases. Contrary to the two-phase architecture, the CDTI gates must be at high state, thereby un-passivated, when carrying signal. However, if the line rate is fast enough (e.g. 1 MHz implies a sub-microsecond high state) the feature of dynamic surface passivation can be retrieved. Moreover, if charge storage is performed under one phase (S1) instead of two phases (S2), the high-state period can be reduced further by a factor of two. Although, this is at the expense of the FWC which is also divided by two.

CTI results are shown in Fig. 9 with charge storage under one (4P4G-S1) and two phases (4P4G-S2) at 100 kHz, which enables a comparison with the two-phase CTI in Fig. 4. In both cases, the minimum CTI is better than in the 2P4G-T0 case, but this can be attributed to the use of a longer transfer time. In the 4P4G-S2 case, the FWC is twice the S1's as expected, but a severe CTI issue occurs which cause remains so far unknown. Overall, it is currently impossible to conclude on the possible benefits brought by a four-phase architecture, but the early results are promising.

V. Conclusion

In conclusion, the presented designs and first electrical tests confirm the strong potential of CDTI CCD-on-CMOS for high line rate and high dynamic range applications. Improvements in CTI at 100 kHz are obtained with both 2P4G-T and 4P4G designs. The benefits appear strong for large pixels, which can make a difference in TDI Earth observation. Moreover, multi-MHz charge transfer in the trapeze designs seems within reach, paving the way for machine vision applications. Parasitic interface charge recombination has been examined and appears negligible thus far. However, investigating the 4P4G remains crucial in the purpose of comparing the buried channels. The performances of the studied 2P4G and 4P4G 12 µm pixels are summed up in Table I and compared with the CCD-on-CMOS state-of-the-art. Further improvements are expected by optimizing the readout chain with multiplexing options [4], for example, with a skipper architecture [8].

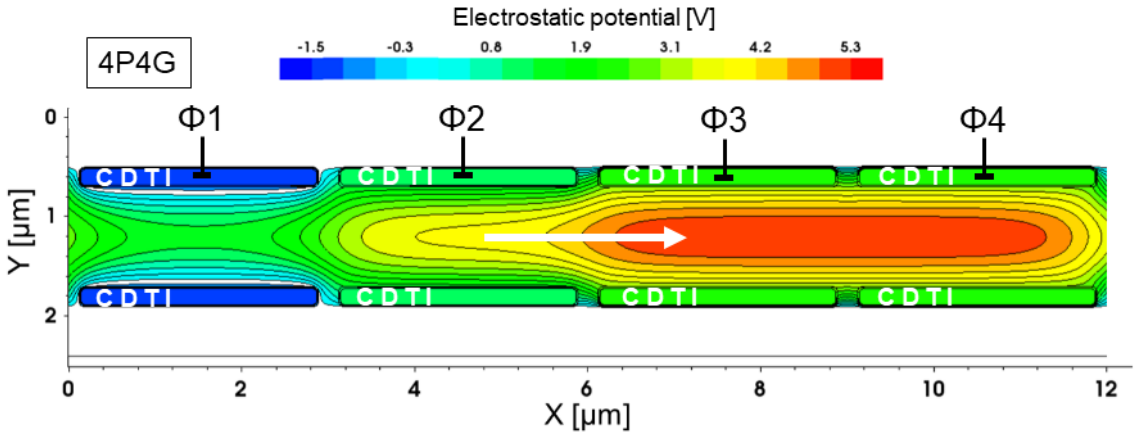

Fig. 8: Top view of the potential map of a 4-phases 4-gates (4P4G) pixel structure in charge transfer condition. In this simulation, $\Phi 1 = -1$ V, $\Phi 2 = 1.5$ V, $\Phi 3 = 3$ V and $\Phi 4 = 3$ V.

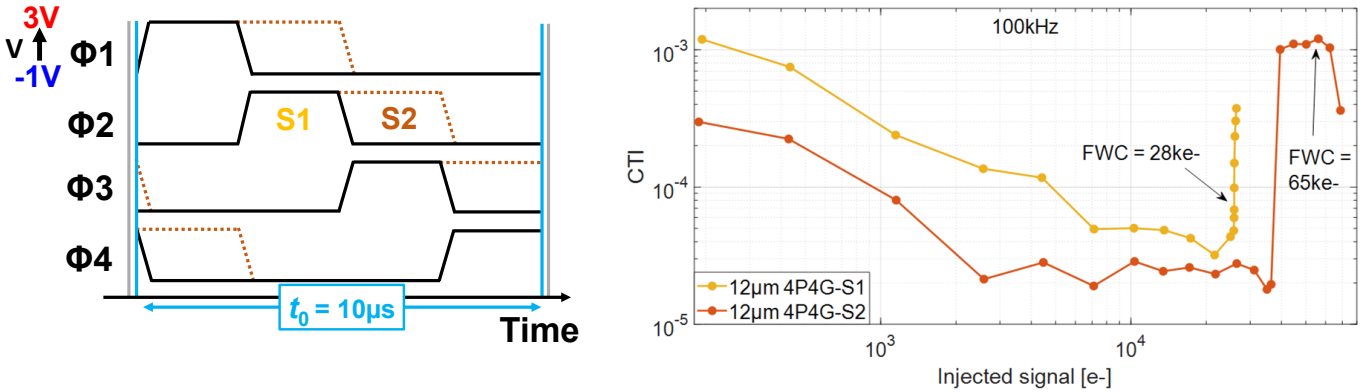

Fig. 9: On the left is a 4P4G clocking diagram with charge storage under one phase (S1) or two phases (S2). On the right, the CTI in a 12 µm 4P4G device is measured versus the injected signal in S1 and S2 modes.

Table. 1 : Performance recap and comparison with the state-of-the-art of CCD-on-CMOS.

	2P4G-**T0** PW=1000ns	2P4G-**T0** PW=100ns	2P4G-**T2** PW=100ns	4P4G-S1	[4]	[8]
Nb. pixels	220	220	220	220	256	256
Pixel pitch [µm×µm]	3×12	3×12	3×12	3×12	2×5	5.4×5.4
Nb. phase	2	2	2	4	4	4
Line rate [kHz]	100	100	100	100	Up to 3000	Up to 200
Minimum CTI	**2×10^{-5}**	**5×10^{-5}**	**7×10^{-6}**	**3×10^{-5}**	$< 10^{-5}$	$< 10^{-5}$
Full well charge [ke-]	70	70	68	28	> 60	LG 12.8 / HG 31.6
Dark current [nA/cm^2]	**0.13**	**0.025**	**0.025**		< 4	5.6
Noise [e-]	5.6	5.2	5.2		20	LG 10 / HG 40
Dynamic range [dB]	81.9	82.6	82.3		69.5	LG 62 / HG 60

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